a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and [The multi layer integrated circuit capacitor of claim 1 further comprising] a plurality of controlled collapse chip connection (C4) lands fabricated on and contacting the third insulator layer and in electrical contact with the plurality of conductive vias.

4. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, [The multi layer integrated circuit capacitor of claim 1] wherein at least one of the conductive layers comprise a metal material and at least one of the insulator layers comprise $BaSrTiO_3$.

6. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer;

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers; and [The multi layer integrated circuit capacitor of claim 1 further comprising] a fourth conductive layer located over the third insulator layer, the fourth conductive layer being patterned to form interconnect lines that selectively connect the plurality of conductive vias.

7. (Amended) A multi layer integrated circuit capacitor comprising:

a substrate;

a first conductive layer located over and contacting the substrate;

a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;

a second conductive layer located over the first insulator layer;

a second insulator layer located over the second conductive layer;

a third conductive layer located over the second insulator layer;

a third insulator layer located over the third conductor layer; and

a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, [The multi layer integrated circuit capacitor of claim 1] wherein the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

REMARKS

The Applicant's representative has carefully reviewed and considered the Office Action mailed on October 24, 2002, as well as the references cited therewith. Claims 1 and 8 have been canceled. Claim 2, 4, 6, and 7 have been amended to incorporate canceled base claim 1, and not for reasons related to patentability. No claims are added. As a result, claims 2-7 and 9-21 are now pending in this Application.